Monolithic Fringe-Field-Activated Crystalline Silicon Tilting-Mirror Devices

Dennis S. Greywall, Chien-Shing Pai, Sang-Hyun Oh, Chorng-Ping Chang, *Senior Member, IEEE*, Dan M. Marom, Paul A. Busch, Raymond A. Cirelli, J. Ashley Taylor, Fred P. Klemens, Thomas W. Sorsch, John Eric Bower, Warren Y.-C. Lai, *Member, IEEE*, and Hyongsok T. Soh, *Member, IEEE, Member, ASME*

***Abstract*—A new approach is presented for fabricating monolithic crystalline silicon tilting-mirror microoptoelectromechanical systems (MOEMS) devices. The activation electrodes, etched from a thick silicon layer deposited over insulating oxide onto the top surface of a silicon-on-insulator (SOI) wafer, are displaced from the mirrors and interact with these tilting elements via electrostatic fringing fields. In contrast to the more usual parallel-plate activation, the rotation angle saturates at high voltages. This paper discusses concept, design, and processing, and also compares modeling and measured performance of a specific 9° tilt range device array. [977]**

***Index Terms*—MEMS, MOEMS, micromachined structures, optical telecommunications.**

I. Introduction

MICROMACHINED silicon tilting mirrors have found application in a wide variety of optical devices such as projectors and beam scanners [1] and as switching elements in optical communications components (optical cross connects, [2]–[4] wavelength blockers [5] and sorting switches [6], add-drop switches, [7], etc.). The physical design of these microopticalelectrical mechanical systems (MOEMS) devices differs widely, constrained not only by the requirements of a particular application but also by the fabrication method. For example, mirrors [8] fabricated using a multilevel polysilicon process usually require some type of assembly mechanism to displace the mirrors away from the underlying substrate (to increase the motion range), while crystalline mirrors [2], [9] fabricated using two-sided etching of silicon-on-insulator (SOI) wafers require a precisely aligned bonding to a second electrode wafer.

Merits of the SOI process are that: i) it allows separate fabrication of the mechanical and electrical components of the device; ii) it allows large latitude for mirror thickness and gap spacing between mirrors and electrodes; iii) it allows large mirror fill factors; and iv) it allows simpler mechanical structures. These advantages of the two-piece approach can be utilized, e.g., for large-mirror, large-port cross-connect switches where mirror size and fill factor and wire routing are significant issues. However, for small mirror devices (e.g., wavelength blockers and wavelength sorting switches) alignment tolerances can become unmanageably tight.

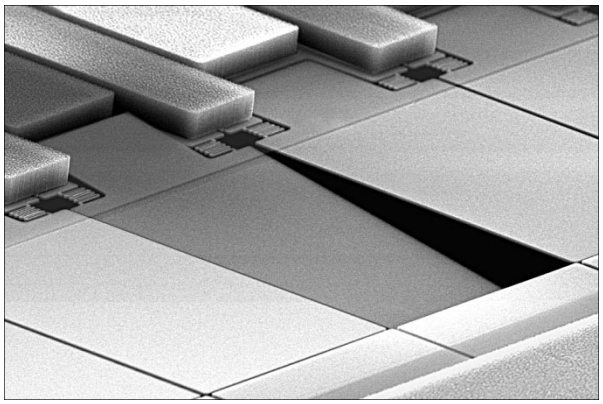


Fig. 1. SEM image showing a linear array of 80 μm-wide MEMS mirrors with one element rotated 7°. The mirrors are made of crystalline silicon and are covered with a thin layer of aluminum. The relatively thick, deposited polysilicon layer is used to pattern the electrodes and the ground shields. The electrodes are longitudinally offset from the mirrors and interact with the mirrors via electrostatic fringing fields.

A common problem with both the multilayer polysilicon and the SOI processes stems from the use of parallel-plate electrostatic actuation. An intrinsic characteristic of this actuation is that a small overvoltage can cause a mirror to snap abruptly into contact with the underlying substrate. Aside from the possible mechanical and electrical damage, a simple touch can also cause the two surfaces to stick together permanently. A further problem, especially for switching applications that require stability, is that exposed dielectrics can charge and cause mirror tilt drift with time. There can also be issues with electrical or mechanical cross talk between neighboring mirrors.

This paper discusses a significant improvement of the SOI process that can be implemented in various manners and that remedies many problems of earlier fabrication schemes. In particular, the new MOEMS structures are monolithic, do not exhibit rotational snapdown, have electrical shielding between channels, and have activation voltages less than or comparable to parallel plate devices. The approach [10] is discussed in terms of an application requiring a linear array of closely spaced cantilever mirrors. See the SEM micrograph in Fig. 1 and the corresponding schematic drawing in Fig. 2.

The basic idea is to use thick polysilicon electrodes located on top of the SOI layer but offset from the mirror elements.

Manuscript received December 16, 2002; revised June 15, 2003. Subject Editor T. Kenny.

D. S. Greywall, C.-S. Pai, P. A. Busch, R. A. Cirelli, J. A. Taylor, F. P. Klemens, T. W. Sorsch, J. E. Bower, and W. Y.-C. Lai are with Bell Laboratories, Lucent Technologies, Murray Hill, NJ 07974 USA (e-mail: dsgrey@lucent.com).

S.-H. Oh, C.-P. Chang, and H. T. Soh are with the MEMS R&D Group, Agere Systems, Berkeley Heights, NJ 07922 USA.

D. M. Marom is with Bell Laboratories, Lucent Technologies, Holmdel, NJ 07733 USA.

Digital Object Identifier 10.1109/JMEMS.2003.818068

1057-7157/03$17.00 © 2003 IEEE

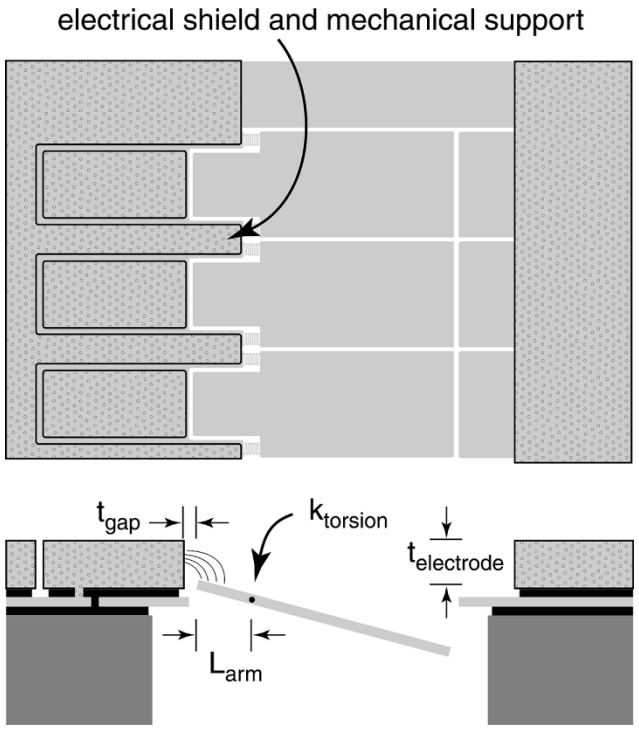


Fig. 2. Schematics showing top and cross-sectional views of a linear array of tilting mirrors with fringe-field activation. Various parameters are defined.

The three-dimensional (3-D) electrode geometry allows a significant electrostatic interaction between the nearly horizontal mirror plate and the vertical face of the bulk electrode, leading to mirror tilting. The structure is referred to as a fringe-field (FF) activated device. In addition to its being used to create the electrodes, the polysilicon layer also serves to stiffen the support for the torsional springs, to provide electrical shielding between channels, and to create a grounded capping for the traces etched into the SOI layer.

Sections II–IV outline the FF processing, summarize the modeling performed for a particular device geometry, and present test results that validate the simulations.

II. Processing

The starting wafer consists of an SOI substrate with a top crystalline silicon thickness of 1 μm. First, the mirrors and springs, see Fig. 2, are patterned into the SOI layer using DUV lithography and silicon RIE (reactive ion etch) techniques in order to achieve the required submicron critical-dimension control. Next, a thin insulating dielectric film is deposited and patterned with small contact holes. Finally, the structure is covered with the 10 μm-thick *in situ*-doped CVD polysilicon layer used to create the thick electrodes.

Since the physical profile of the electrodes has a critical impact on device operation, deep RIE with alternating etch/deposition steps is used to create nearly vertical sidewalls, as shown in Fig. 3. The horizontal barring in the SEM micrograph is a marker of the DRIE process; the vertical striations are a mapping of the texture of the top surface of the thick polysilicon layer that was left unpolished. Fig. 4 is a similar image but now showing a polysilicon electrode in relation to the actuator arm

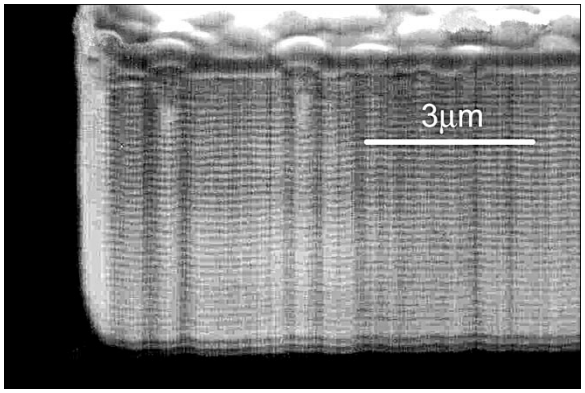


Fig. 3. SEM micrograph showing the vertical sidewall of an electrode.

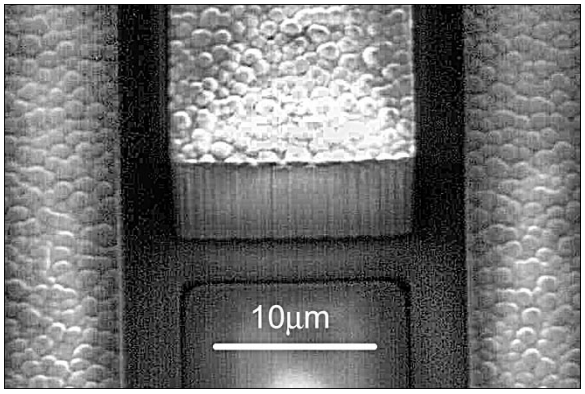


Fig. 4. SEM showing the 3-D electrode in relation to the actuator arm of the tilting mirror. This device has 3 μm gaps on either side of the electrode.

of an SOI mirror. For this particular device the trench on either side of the electrode is 3 μm wide and free of residues that could cause electrical shorts. The gap spacing $t_{\rm gap}$ between the electrode face and the end of the actuator arm is also accurately 3 μm.

Once the front side processing is completed, the handle is deep etched from the backside of the substrate to create the cavity under the mirrors that allowes significant out-of-plane motion. The oxide layers are removed to release the mirrors and the springs using an HF etch and a CO_2 critical point dryer. Metal is evaporated onto the mirror surface using a shadow mask.

III. Modeling

A MEMS structure consisting of a movable plate and an underlying parallel electrode often can be modeled quite accurately using the simple parallel plate approximation. This is not the case, however, for the device shown in Fig. 1, since the electrode is now laterally offset from the tilting element and the electrostatic interaction is determined totally by the fringing fields, i.e., the very contributions that are usually ignored in analytic modeling. Instead, it was necessary to estimate the fringe-field interactions using 3-D numerical simulations. To simplify the computations, the assumption was made, consistent with our design goals, that the rotational and translational components of the mirror's response to the applied voltage could be treated independently.

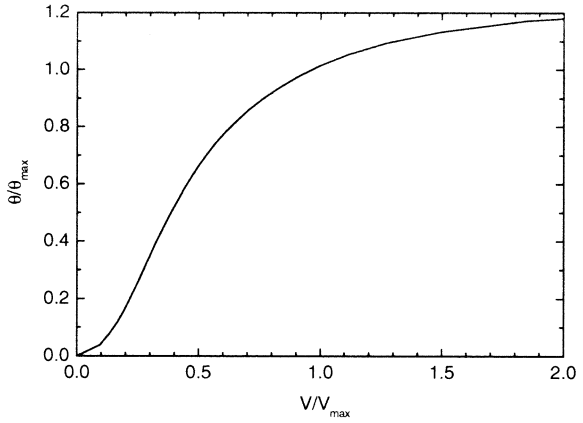


Fig. 5. Reduced plot of angle versus voltage.

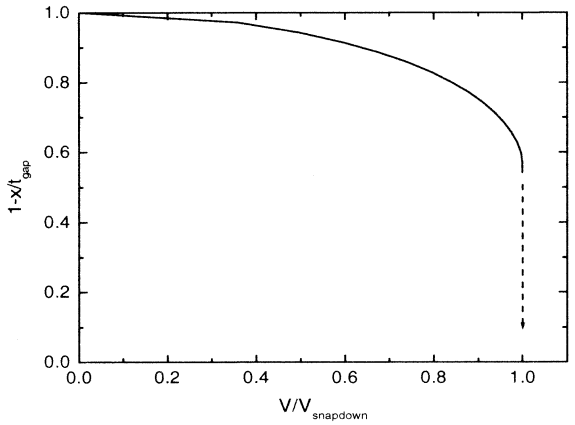


Fig. 6. Reduced plot of longitudinal displacement versus voltage.

Equating the electrostatic torque T_e, given by the derivative of the stored energy with respect to angle

$$T_e = \frac{d}{d\theta}\left(\frac{CV^2}{2}\right) = \frac{V^2}{2}\frac{dC}{d\theta} \tag{1}$$

to the mechanical torque

$$T_m = k_{\text{torsion}}\theta \tag{2}$$

yields the expression

$$\frac{1}{\theta}\frac{dC}{d\theta} = \frac{2k_{\text{torsion}}}{V^2} \tag{3}$$

that relates rotation angle to applied voltage. The calculation therefore reduces to a determination of the angular dependence of the capacitance derivative. This estimate was made by numerically computing the capacitance between the electrode and the surrounding grounded components of the structure over a set of finely spaced, fixed rotation angles. The entire analysis was repeated over a multidimensional grid with $2 < t_{\text{gap}} < 8\ \mu\text{m}$, $20 < L_{\text{arm}} < 60\ \mu\text{m}$, $10 < w_{\text{electrode}} < 60\ \mu\text{m}$, and $5 < t_{\text{electrode}} > 30\ \mu\text{m}$. Other physical parameters describing the details of the chosen geometry were held fixed. See Fig. 2.

It was found that all of the modeling results could be described well by the universal plot shown in Fig. 5 with the normalizing factors $\theta_{\max}$ and $V_{\max}$ given by the empirical functions

$$\theta_{\max} \approx \frac{36.2t_{\text{gap}}^{1/3}}{L_{\text{arm}}^{1/2}}\left(1 - e^{-t_{\text{electrode}}/4.7}\right) \tag{4}$$

and

$$V_{\max} \approx 600t_{\text{gap}}\sqrt{\frac{\frac{k_{\text{torsion}}}{10^{-11}}}{w_{\text{electrode}}L_{\text{arm}}}} \tag{5}$$

with lengths measured in microns and k_{torsion} in MKS units.

Translation of the mirror was treated in an analogous manner, but with force and displacement replacing torque and angle. Here it was determined that at sufficiently high voltage there will be a longitudinal snap down. These modeling results can be represented in terms of the reduced plot shown in Fig. 6 and the relation

$$V_{\text{snapdown}} \approx 190t_{\text{gap}}\sqrt{\frac{k_{\text{linear}}}{w_{\text{electrode}}}}. \tag{6}$$

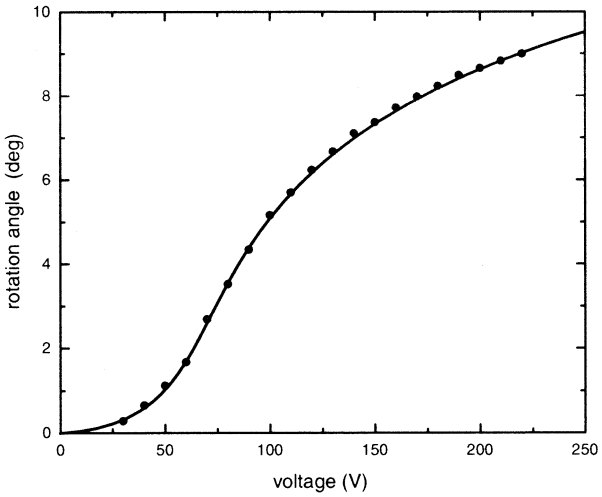


Fig. 7. Measured rotation angle as a function of activation voltage.

Instability occurs when the displacement reaches roughly 40% of the initial gap spacing t_{gap}.

Once the expressions for $\theta_{\max}$, $V_{\max}$, and V_{snapdown} were determined, it was straightforward to design for a specific application. As an example: Within the range of reasonable physical values for the parameters $t_{\text{gap}}, L_{\text{arm}}, w_{\text{electrode}}$, and $t_{\text{electrode}}$ and for the dimensions of the torsional springs, it was possible to have $\theta_{\max} \approx 9.2°$, $V_{\max} \approx 175$ V, and $V_{\text{snapdown}} \approx 300$ V. Fig. 5 and these scaling parameter values then indicate that a working angle of 6.5° is reached at about 100 V. Fig. 6 shows that at 100 volts there is very little compression of the spring, justifying the separation of rotation and translation in the modeling.

An analysis of the vibrational modes of the structure gave a fundamental frequency of 3.8 kHz and placed the next higher frequency mode at 40 kHz. A simple estimate indicated that the cantilever tilt due to gravity is smaller than 0.01°.

IV. Experimental Results

The behavior measured for the device described in the previous paragraph is shown in Fig. 7. The overall shape of the response is in excellent agreement with the modeling curve, but

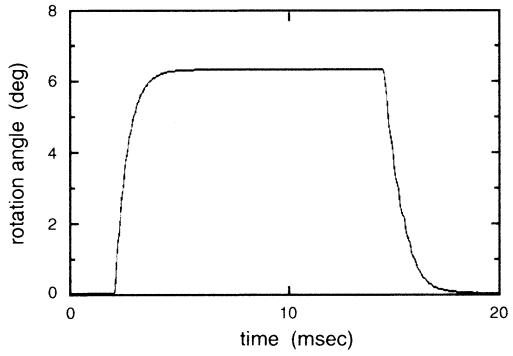


Fig. 8. Response to a 150-V square-wave pulse. The rise time of the filtered response is of the order of 1 ms.

the rotation of 6.5° is reached at about 130 V. The 30% discrepancy is explained by the SEM measured width of the torsional spring elements being larger than the layout value of 0.5 μm. At an activation of 270 V, a measurable leakage current was detected, but there was still no evidence of linear snapdown.

The measured frequency response showed a resonance at 4 kHz, as expected, with a Q of about 5 at atmospheric pressure. This underdamping means that there will be ringing associated with a square-wave activation of the mirrors, but the ringing will extend out only for a few milliseconds. The amount of mechanical ringing can be reduced by adjusting the rise and fall times of the drive signal or can be completely hidden, as shown in Fig. 8, by using a low pass filter on the photodetector receiving the reflected light. Running the square wave drive with periods of 200 seconds showed no evidence of mirror tilt drifting.

V. Conclusion

We have demonstrated a novel, manufacturable process for fabricating monolithic, crystalline silicon, tilting-mirror devices. The devices incorporate fringe-field electrostatic activation and do not undergo snapdown. The actuation principle and the processing scheme can be applied to a wide range of MEMS devices.

Acknowledgment

The expert advice and/or technical assistance of the following are gratefully acknowledged: G. Bogart, E. Ferry, A. Kornblit, D. Lopez, B. Mansfield, J. Miner, S. Rogers, M. Schlax, and K. Werder.

References

[1] P. F. Van Kessel, L. J. Hornbeck, R. E. Meier, and M. R. Douglass, "A MEMS-based projection display," *Proc. IEEE*, vol. 86, p. 1687, Aug. 1998.

[2] D. S. Greywall, P. A. Busch, F. Pardo, D. W. Carr, G. Bogart, and H. T. Soh, "Crystalline silicon tilting mirrors for optical cross connect switches," *J. Microelectromech. Syst.*, vol. 12, pp. XXX–XXX, Oct. 2003.

[3] D. J. Bishop, C. R. Giles, and S. R. Das, "The rise of optical switching," *Scientif. Amer.*, pp. 88–94, Jan. 2001.

[4] J. H. Smith, S. S. Nasiri, J. Bryzek, M. Novack, J. B. Starr, H. Kwon, A. F. Flannery, D. L. Marx, Z. Chen, and D. Sigari, "1200 mirror array integrated with CMOS for photonic switching: Application of mechanical leveraging and torsional electrostatic actuation to reduce drive voltage requirements and increase angular tilt," in *Solid-State Sensor, Actuator and Microsystems Workshop*, Hilton Head Island, SC, June 2–6, 2002, p. 378.

[5] D. T. Neilson *et al.*, "High-Dynamic range channelized MEMS equalizing filter," in *OFC 2002 Tech. Dig.*, Mar. 2002, p. 586.

[6] D. M. Marom, D. T. Neilson, D. S. Greywall, N. R. Basavanhally, P. R. Kolodner, Y. L. Low, F. Pardo, C. A. Bolle, S. Chandrasekhar, L. Buhl, C. R. Giles, S.-H. Oh, C. S. Pai, K. Werder, H. T. Soh, G. R. Bogart, E. Ferry, F. P. Klemens, K. Teffeau, J. F. Miner, S. Rogers, J. E. Bower, R. C. Keller, and W. Mansfield, "Wavelength-selective 1 × 4 switch for 128 WDM channels at 50 GHz spacing," in *Optical Fiber Conf. (PD FD7)*, Anaheim, CA, 2002.

[7] J. E. Ford, V. A. Aksyuk, D. J. Bishop, and J. A. Walker, "Wavelength add-drop switching using tilting micromirrors," *J. Lightwave Technol.*, vol. 17, p. 904, May 1999.

[8] V. A. Aksyuk, F. Pardo, D. Carr, D. Greywall, H. B. Chan, M. E. Simon, A. Gasparyan, H. Shea, V. Lifton, C. Bolle, S. Arney, R. Frahm, M. Paczkowski, M. Haueis, R. Ryf, D. Neilson, J. Kim, R. Giles, and D. Bishop, "Beam-Steering micromirrors for large optical crossconnects," J. Lightwave Technol., to be published.

[9] D. S. Greywall, "Process for Fabricating an Optical Mirror Array," U. S. Pat. 6 201 631.

[10] C. A. Bolle and E. Chan, private communication, 2000.

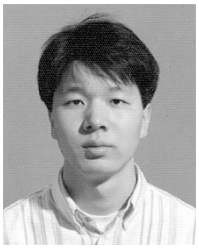
Dennis S. Greywall received the B.S. degree in physics from the University of Detroit, MI, in 1965 and the Ph.D. degree in low-temperature physics from Indiana University in 1970. Immediately thereafter, he joined Bell Laboratories, Murray Hill, NJ.

His work has included experimental studies of helium crystals, superfluidity in 3He and 4He, and magnetism in two-dimensional 3He. He has also worked on noise evasion and on mechanical dissipation in very small systems at very low temperatures. Since 1995, his focus has been on the mechanical design and modeling of MOEMS devices such as modulators, cross connects, and wavelength sorting switches. In addition, he has designed MEMS-based RF filters, *in vivo* medical devices, and adaptive optics mirrors.

Dr. Greywall is a Distinguished Member of Technical Staff at Bell Laboratories, a Fellow of the American Physical Society, and was the recipient of the 1993 London Prize in Low Temperature Physics.

Chien-Shing Pai received the B.S. degree in electrophysics from Chiao-Tung University, Hsin-Chu, Taiwan, in 1978 and the Ph.D. degree in electrical engineering from the University of California, San Diego in 1985.

Since 1985, he has been working at Bell Laboratories, Murray Hill, NJ, in the area of Advanced Electronic Device Research. He was involved in research and development in both device and processing for advanced CMOS technologies for ULSI applications. His work included selective-epi and silicide for front-end CMOS device and low-k materials and multilevel-interconnect integration for sub-100 nm ULSI applications. In 2000, his work expanded to include MEMS technology for communication and biotech applications. He is a Distinguished Member of Technical Staff at Bell Laboratories. He has served as committee member in VLSI Technology Symposium since 1996 and has organized and chaired short course and rump session for several years.



Sang-Hyun Oh received the B.S. degree in physics from the Korean Advanced Institute of Science and Technology (KAIST), Korea, in 1996 and the Ph.D. degree in applied physics from Stanford University, Stanford, CA, in 2001. His doctoral work was on the design and fabrication of nanoscale CMOS transistors.

He joined the MEMS R&D group at Agere Systems in 2001, where he was engaged in the design of optical MEMS devices such as cross-connects, dynamic gain equalizers, and wavelength sorting switches. From 1998 to 2000, he worked at Bell Laboratories, Murray Hill, NJ, where he focused on developing novel sub-50 nm vertical transistors. He is now an Advisory Engineer at IBM Microelectronics in East Fishkill, NY, where he is developing high-performance 90-nm logic technology.

Chorng-Ping Chang (M'97–SM'01) received the B.S. degree in nuclear engineering from the National Tsing Hua University, Hsu-Chu, Taiwan, in 1978 and the Ph.D. degree in nuclear fusion and plasma physics from the University of California at Berkeley in 1985.

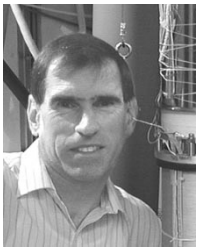
In the same year, he joined AT&T Bell Laboratories (which later became Lucent Technologies Bell Laboratories), Murray Hill, NJ, engaging in research and development activity on advanced plasma processing, front-end CMOS process integration, novel sub-50 nm device fabrication and silicon MEMS for telecommunication applications. Currently, he works for New Jersey Nanotechnology Consortium, the spin-off of Bell Laboratories nanofabrication facility.

Dr. Chang is a Senior Member of IEEE Electron Devices Society. He had served on the Device and Interconnect Technology subcommittee and the Process Technology subcommittee for IEEE IEDM (International Electron Devices Meeting). He has been an Editor of IEEE ELECTRON DEVICE LETTERS since 2000, specialized in silicon device and technology.

Dan M. Marom received the B.Sc. degree in mechanical engineering and the M.Sc. degree in electrical engineering, both from Tel-Aviv University, Israel, in 1989 and 1995, respectively, and the Ph.D. degree from University of California, San Diego (UCSD) in 2000. In his doctoral dissertation, he investigated femtosecond-rate optical signal processing with applications in ultrafast communications.

From 1996 through 2000, he was a Fannie and John Hertz Foundation Graduate Fellow at UCSD. In 2000, he joined the Advanced Photonics Research Department at Bell Laboratories, Lucent Technologies, where he is working on novel MEMS based switching solutions using MEMS technology for optical communications.

Dr. Marom received the IEEE Lasers and Electro-Optics Society best student paper award in 1999 for his work describing instantaneous time reversal of complex amplitude ultrafast waveforms.



Paul A. Busch received the B.S. degree in physics from Upsala College in 1972.

He then joined the Physical Research Laboratory at Bell Laboratories, Murray Hill, NJ. His work has included studies in condensed matter physics at ultralow temperatures and the mechanical testing of prototype MEMS devices.

Raymond A. Cirelli is currently a Senior Member of Technical Staff at Lucent Technologies, Bell Laboratories, Murray Hill, NJ. He has authored over 70 technical papers and has been awarded numerous patents in the field of optical lithography. He has made critical contributions to various aspects of deep-ultraviolet lithography in the areas of; off-axis illumination, reflectivity control, and proximity effect correction. The current emphasis of his work is in new lithography techniques for MEMS and optical waveguide research.

J. Ashley Taylor received the Ph.D. degree physical chemistry at the University of Houston, TX, studying photoionization of gaseous molecules.

As a Postdoctoral Fellow, also at the University of Houston, he investigated the reactions of ions with surfaces. He then joined Perkin-Elmer, Physical Electronics Division conducting surface analysis (XPS and Auger) for many different applications. In 1984, he joined AT&T Bell Laboratories, Allentown, PA, where he conducted many different studies characterizing materials used for the manufacturing of integrated circuits. In 1994, he moved to Orlando, FL, to develop dielectric plasma etch processes for the VLSI Process Development Department. In 1997, he was assigned to SEMATECH in Austin, TX, as the Project Manager for the Damascene Dielectric Etch Project. During that time he established joint projects with various plasma etch vendors and negotiated the placement of plasma etch tools at SEMATECH for evaluation of etching low-k dielectric materials. In 1997, he returned to Orlando, FL, to continue his work in developing plasma etch processes for low-k dielectric materials, which was an important part in the development of the 0.13 μm integrated-circuit technology. In 2002, he moved to Murray Hill, NJ, to work for Agere Systems and then for Lucent Technologies, Bell Laboratories, developing processes for deep silicon plasma etch for optical MEMS devices. Recently, he has been studying the interaction of liquids with nanotextured silicon surfaces. He has authored more than 30 publications dealing with materials characterization and plasma etch and has several patent applications pending.

Fred P. Klemens, photograph and biography not available at the time of publication.

Thomas W. Sorsch, photograph and biography not available at the time of publication.

John Eric Bower received the Ph.D. degree in physics from the Stevens Institute of Technology, Hoboken, NJ, in 1993.

Following the completion of his undergraduate physics degree at Pennsylvania State University, he was employed by Chemcut Corporation, Nuclide Corporation, Instruments SA, and Arthur D. Little, Inc., where he worked in a number of fields, including mass spectrometry, atomic emission spectroscopy, and Molecular Beam Epitaxy. He did graduate work at Pennsylvania State University and Northeastern University prior to coming to Bell Laboratories in 1985, where he has worked in the Atomic Cluster, Integrated Circuit, and Nanotechnology fields. He has authored or coauthored more than 50 publications and has two patents.

Warren Y.-C. Lai (M'82) received the Ph.D. degree in physics from the California Institute of Technology, Pasadena, in 1980, working in low-temperature physics. He then joined Bell Laboratories, Murray Hill, NJ, doing research and development in silicon microelectronics technology, optical MEMS technology and nanotechnology. His work in silicon multilevel interconnect technology for CMOS covered Al multilevel interconnect (including CVD Al and laser planarization), CVD W plug, chemical mechanical planarization, Cu-dual damascene, low-k dielectric for IC, and high-k dielectric for embedded DRAM. In late 2000, his work extended to optical MEMS including SOI-based optical cross connect. Since mid–2002, he worked in nanofabrication research and helped to form the New Jersey Nanotechnology Consortium (NJNC).

Dr. Lai is a Distinguished Member of Technical Staff at Bell Laboratories. He is a Member of the APS and serves on the Program Committee of IEEE IITC (International Interconnect Technology Conference).

Hyongsok T. Soh (M'02) received the B.S. degree with distinction with a double major in mechanical engineering and materials science from Cornell University, Ithaca, NY, in 1992, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1995 and 1999, respectively.

He served as the Technical Manager of MEMS device research group at Bell Laboratories and MEMS R&D group at Agere Systems before joining the University of California-Santa Barbara in 2003 as an Assistant Professor in Mechanical Engineering. His research interests include scanning probe devices and techniques, use of MEMS technology for nanometer scale detection and manipulation, and parallel operation of micromachined devices. He has (co)authored over 25 technical papers, 10 patents, and one book.

Dr. Soh is a Member of the American Society of Mechanical Engineers (ASME).